REMARKS

This preliminary amendment is submitted with a Request for Continued Examination in the above-identified application. In view of the final Office Action dated February 1, 2005, applicant takes this opportunity to present the following remarks and the amendments set forth above.

Specifically, in the final Office Action, the Examiner rejected claims 1-7 as being unpatentable over U.S. Patent No. 5,101,128 to Butler. The Examiner argues that Butler shows an amplifier circuit that has two transistors and wherein the threshold voltage implants of the transistors J1 and J2 produce controlled offsets at the output of the amplification stage.

Applicant has reviewed the cited reference and has determined that Butler describes an amplifier front end made up of two differential pairs driven in parallel. The amplifier of Butler uses the two pairs to provide different values of transconductance g_m in different regions of the input signal range. Close to balance (where the total current into the first stage load is equal on both sides of the composite front end), one pair of bipolar transistors provide a high transconductance g_m. Away from balance where the transconductance of the bipolar transistor pair has fallen to near zero due to the large input signal, another pair of transistors provides a transconductance g_m that is less than the bipolar transistor pair near balance but more than the bipolar transistor pair in the large signal region.

Importantly, if one of the pairs is made with an overt offset as the Examiner suggests, there would indeed be an offset to the balance point of the input stage. However, the offset would be partly due to each pair and would inhibit drift with temperature and unpredictable variations across the manufacturing production spread. For example, assuming that Butler's high transconductance pair is made with bipolar transistors and a low transconductance pair is made with MOSFETs and that the MOSFET pair is made with a controlled offset of 0.5 volts. Depending upon the relative values of the

tail currents in each pair, the balance point could be shifted from near zero to nearly 0.5 volts. Even though the current in the first stage load would be balanced, the currents in both input pairs would be unbalanced, i.e., the left bipolar transistor would have a different current from that in the right bipolar transistor. A similar situation would exist for the MOSFETs.

Thus, by implementing an offset as the Examiner suggests, the output offset would drift with temperature and the initial value of the offset would depend not only on the process that induced the controlled offset in the MOSFET pair but also in the variation in the ratio of the two tail currents. Therefore, there is not a suggestion to modify the structure shown in the Butler patent with a controlled offset as taught in the present invention. If this were done with the Butler circuit, this would result in an inoperable circuit.

The present claimed invention contemplates that the MOS transistors in the input pair are running at the same current and that there is negligible drift with temperature and across the production spread of the manufacturing process. As seen in Figure 1, a current source 105 feeds both of the input transistors. The claims have been amended to recite such a limitation and thus are now believed to be in condition for allowance.

The Examiner argues that Figure 2 of the Butler patent shows an input stage that may have the threshold voltage implants varied to control an offset voltage or that it would be obvious to do so. The Examiner does not point to any teaching in the Butler patent that the input stage has different threshold voltage implants. Instead, the Examiner merely argues that the structural limitations of Butler are the same as the claimed invention and therefore Butler has the capability to perform the claimed functional limitations.

Applicant disagrees with the Examiner's assertion and interpretation of the current state of the law. First, the structure of Butler is not the same as the structure of the claimed invention. In Butler, the transistors J1 and J2 are matched to one another and there is no indication that there is any significant or intentional difference in their characteristics. Indeed, a typical input stage would have matched transistors.

In contrast, the present claimed invention **uses transistors that are purposefully not matched**. One of the transistors has a different threshold implant, and in one embodiment, may have no threshold implant. It is respectfully submitted that a transistor without a threshold implant is fundamentally a different device than a transistor with a threshold implant. Thus, in claim 1 and in claim 6, the limitation where it states that the two transistors have different threshold voltage implants is not structurally met by the circuit shown in Figure 2 of Butler.

In view of the foregoing remarks, applicant respectfully requests reconsideration and an Issuance of a Notice of Allowance. Should any further questions remain, the Examiner is invited to contact applicant's attorney at the telephone number listed below.

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Respectfully submitted,

By _____

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